WHAT IS CLAIMED IS:

1. An apparatus for evaluating an amount of charge, the apparatus comprising:

a substrate having a substantially intrinsic undoped silicon layer;

p-type regions dotted as discrete islands in the undoped silicon layer; and

a first insulating layer provided over the undoped silicon layer and the p-type regions.

2. The apparatus of claim 1, wherein a second insulating layer is provided in a region of the substrate located below the undoped silicon layer.

3. The apparatus of claim 2, wherein the second insulating layer has a thickness not less than 1 nm and not more than 500 nm.

4. The apparatus of claim 1, wherein the undoped silicon layer has a thickness not less than 10 nm and not more than 10 μm.

5. The apparatus of claim 1, wherein a concentration of an impurity contained in the p-type regions is not less than 1×10^{16} cm^{-3} and not more than 1×10^{23} cm^{-3}.

6. The apparatus of claim 1, wherein a concentration of an impurity contained in the undoped silicon layer is not more than 1×10^{15} cm^{-3}.

7. The apparatus of claim 1, wherein the first insulating film has a thickness not less than 1 nm and not more than 500 nm.

8. The apparatus of claim 1, further comprising:

a third insulating layer composed of an insulating material and provided on a back surface of the semiconductor substrate.

9. The apparatus of claim 8, wherein the third insulating layer has a thickness not less than 1 nm and not more than 500 nm.

10. The apparatus of claim 1, further comprising:

a conductor film on the first insulating layer.

11. An apparatus for evaluating an amount of charge, the apparatus comprising:

a substrate having a silicon layer;

p-type regions each surrounded by the silicon layer, having a valence band edge potential higher than that of the silicon layer, and composed of silicon containing a p-type impurity; and

a first insulating layer provided over the silicon layer and the p-type regions.

12. The apparatus of claim 11, wherein a region of the substrate located under the silicon layer is provided with a second insulating layer.

13. An apparatus for evaluating an amount of charge, the apparatus comprising:

a substrate having a first insulating layer;

p-type regions dotted as discrete islands in the insulating layer and composed of silicon containing a p-type impurity; and

a second insulating layer provided over the first insulating layer and the p-type regions.

14. A method for fabricating an apparatus for evaluating an amount of charge, the method comprising the steps of:

forming a first insulating layer on a substrate;

forming a substantially intrinsic undoped silicon layer on the first insulating layer;

selectively introducing a p-type impurity into the undoped silicon layer and forming p-type regions dotted as discrete islands in the undoped silicon layer; and

forming a second insulating layer over the undoped silicon layer and the p-type regions.

15. A method for evaluating an amount of charge, the method comprising the steps of:

(a) preparing an apparatus for evaluating an amount of charge, the apparatus comprising a semiconductor substrate having a first insulating film on an upper portion thereof, a substantially intrinsic undoped silicon layer provided on the first insulating film, p-type regions each surrounded by the undoped silicon layer and composed of silicon containing a p-type impurity, and a second insulating film provided over the undoped silicon layer and the p-type regions;

(b) performing a specified process with respect to the apparatus for evaluating an amount of charge;

(c) after the step (b), immersing the apparatus for evaluating an amount of charge in an etching solution and etching at least the p-type regions in accordance with a principle of anodization; and

(d) calculating, from an amount of etching in each of the p-type regions, an amount of charge caused by the specified process in the apparatus for evaluating an amount of charge.

16. The method of claim 15, wherein the etching solution used in the step (c) contains ions including those of F atoms.

17. The method of claim 15, wherein the step (d) includes calculating the amount of etching in each of the p-type regions from a change in a weight of the p-type region.

18. The method of claim 15, wherein

the apparatus for evaluating an amount of charge further comprises a back-surface insulating film provided on a back surface of the semiconductor substrate and

the specified process in the step (b) is a back-surface scrubbing process for cleaning the back-surface insulating film.

19. The method of claim 15, wherein the specified process in the step (b) is ion implantation.

20. The method of claim 15, wherein

the apparatus for evaluating an amount of charge further comprises a conductor film provided on the second insulating film and

the specified process in the step (b) is dry etching of the conductor film.